Liuchun Cai

Married, 2 children

Lives in St Paul, MN

Education

M.S. in Electrical Engineering, University of Cincinnati, Ohio (2003)

Ph.D. in Electrical Engineering, University of Minnesota, MN (2009)

Employment after UC Graduation:

2011 – Present: Senior Analog Design Engineer, Micron Technology, Minneapolis, MN
2009 – 2011: Senior ASIC Design Engineer, Data Science International, St. Paul, MN
2007– 2008: RFIC Design Engineer, Honeywell Inc. Minneapolis, MN
2003 – 2007: Graduate School Fellowship, University of Minnesota, Minneapolis, MN

Current Job Description:

Design analog/RF integrated circuits for high speed wideband application.

Publications (**20** journal publications and **10** refereed conference papers)

1. L. C. Cai and P. Boolchand, *Nanoscale Phase Separation of GeS_2 Glass*, Phil. Mag. B 82, 1649 (2002)
2. P. Boolchand, D. Georgieve, F. Wang , T. Qu, L.C. Cai, et.al., *Nanoscale Phase Separation, and Rigidity Transitions in Glasses* C.R. Chimie, 5, 1(2002)
3. R. Harjani and L.C. Cai , *Inductorless Design of Wireless CMOS Frontends*, IEEE ASICON, October 2007
4. L.C. Cai and R. Harjani, *Modeling, Measurement and Mitigation of Crosstalk Noise Coupling in 3D-ICs*, IEEE CICC, Sept. 2008
5. L. C. Cai and R. Harjani, *1-10 GHz Inductorless Receiver In 0.13 um CMOS,* June, RF IC Symposium , 2009
6. L.C. Cai and R. Harjani, *Evaluating Noise Coupling Issues in Mixed-Signal 3D ICs*, Europe Date, April 2009

Email contact: caix0047@umn.edu